SESSION 13 – TAPA I
Multi Gb/s Serial Receivers

Friday, June 18, 1:30 p.m.
Chairpersons: A. Amerasekera, Texas Instruments
C. Kim, Samsung

13.1 — 1:30 p.m.
A 2Gbps and 7-multiplexing CDMA Serial Receiver Chip for Highly Flexible Robot Control System, M. Shiozaki, T. Mukai, M. Ono, M. Sasaki and A. Iwata, Hiroshima University, Hiroshima, Japan

Intelligent robot control systems based on multi-processors, sensors and actuators, require a flexible network for communicating various types of data (e.g. sensor data, interrupt signals). Furthermore, serial data transfer implemented with a few wire lines is also required. For solving the problems, a CDMA serial communication interface utilizing a new two-step synchronization technique is proposed. The receiver chip fabricated in a 0.25um digital CMOS technology achieves a 2Gb/s data-transfer rate and synchronization of 7 multiplex communications.

13.2 — 1:55 p.m.
A 0.11µm CMOS Clocked Comparator for High-Speed Serial Communications, Y. Okaniwa, H. Tamura*, M. Kibune*, D. Yamazaki*, T. Cheung*, J. Ogawa**, N. Tzartzanis**, W.W. Walker** and T. Kuroda, Keio University, Yokohama, Japan, *Fujitsu Laboratories Limited, Kawasaki, Japan, **Fujitsu Laboratories of America, Sunnyvale, CA

A differential comparator targeted at receiving 40 Gb/s signals and operating off a single 1.2V supply was designed and fabricated in 0.11µm CMOS. It comprises a front-end sampler and a regenerative stage with a clocked buffer to achieve a high-speed operation. The clocked buffer employs an impedance modulation technique to reduce the reset time while keeping the effective gain high. We confirmed comparator operation up to 32 Gb/s at a toggle rate of 8GHz.

13.3 — 2:20 p.m.
A 10Gb/s Receiver with Equalizer and On-chip ISI Monitor in 0.11µm CMOS, Y. Tomita, M. Kibune*, J. Ogawa**, W.W. Walker**, H. Tamura* and T. Kuroda, Keio University, Yokohama, Japan, *Fujitsu Laboratories Limited, Kawasaki, Japan, **Fujitsu Laboratories of America, Sunnyvale, CA

A 10Gbps receiver equiped with an equalizer, an ISI monitor and a CDR is proposed and fabricated. The Cherry-Hooper topology is employed to realize an adjustable high-bandwidth equalizer with reduced area and power consumption. The ISI monitor measures the post-cursor and pre-cursor ISI in the equalizer output, using an on-chip correlator. The areas and power consumptions are 47µmx 85µm and 13.2mW for the equalizer and 145µm x 80µm and 10mW for the ISI monitor.

13.4 — 2:45 p.m.
A 2.5-V, 40-Gb/s Decision Circuit Using SiGe BiCMOS Logic, T.O. Dickson, R. Beerkens* and S.P. Voinigescu, University of Toronto, Canada, *STMicroelectronics, Ottawa, Canada

A 40-Gb/s decision circuit is reported which operates from a 2.5-V supply. It includes a flip-flop, a broadband transimpedance preamplifier, a tuned 40-GHz clock buffer, and a 50-ohm output driver. The flip-flop features a novel BiCMOS CML logic topology, which allows for lower supply voltages as compared with pure bipolar implementations without compromising speed. A mm-wave transformer is used to perform single-ended-to-differential conversion along the 40-GHz clock path.

Break 3:10 p.m.